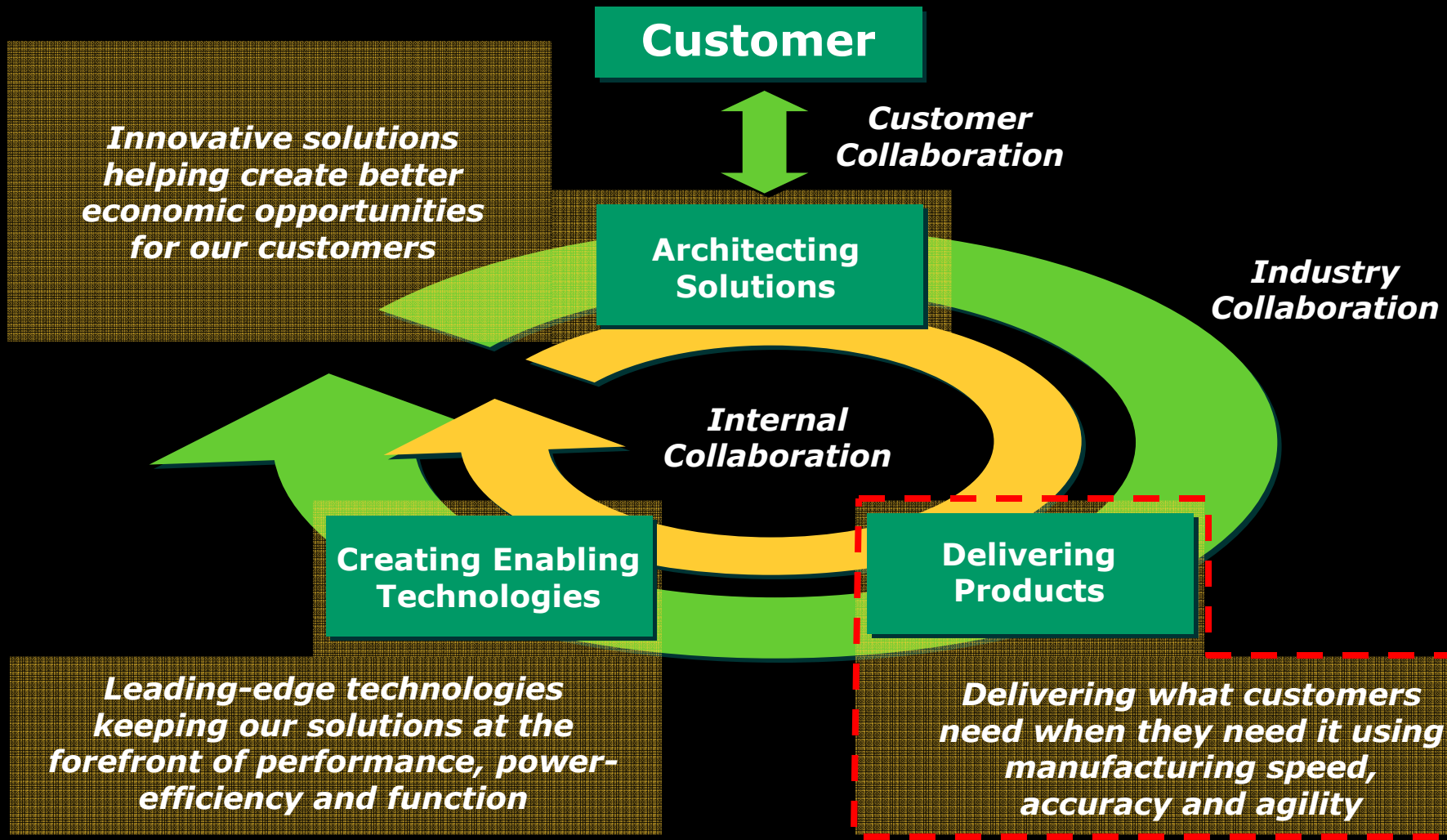
Daryl Ostrander

Senior Vice President,
Logic Technology & Manufacturing,
Product/Technology Implementation,
Microprocessor Solutions Sector
June 10, 2005

Customer-Centric Technology Innovation



Creating an Entirely New Model for *Customer Centric* Manufacturing

AMD has created an entirely *new and differentiated* manufacturing model

It emphasizes speed, accuracy and agility across AMD's manufacturing operations to better respond to, and fulfill, the needs of our customers

We call it Automated Precision Manufacturing (APM)

You can think of it as manufacturing operations deliberately tuned to accurately deliver what customers need, when they need it

Faster customer response

Faster intro of advanced technologies

Better quality and higher efficiencies

Greater capacity flexibility

APM Operational Benefits

Speed + Accuracy + Agility

Rapid product improvements in *current* technology generation

- **Quarterly transistor performance/power upgrades in MPUs — five last year alone**
- **Rapid and consistent increase in production yields on new products in the same technology generation**

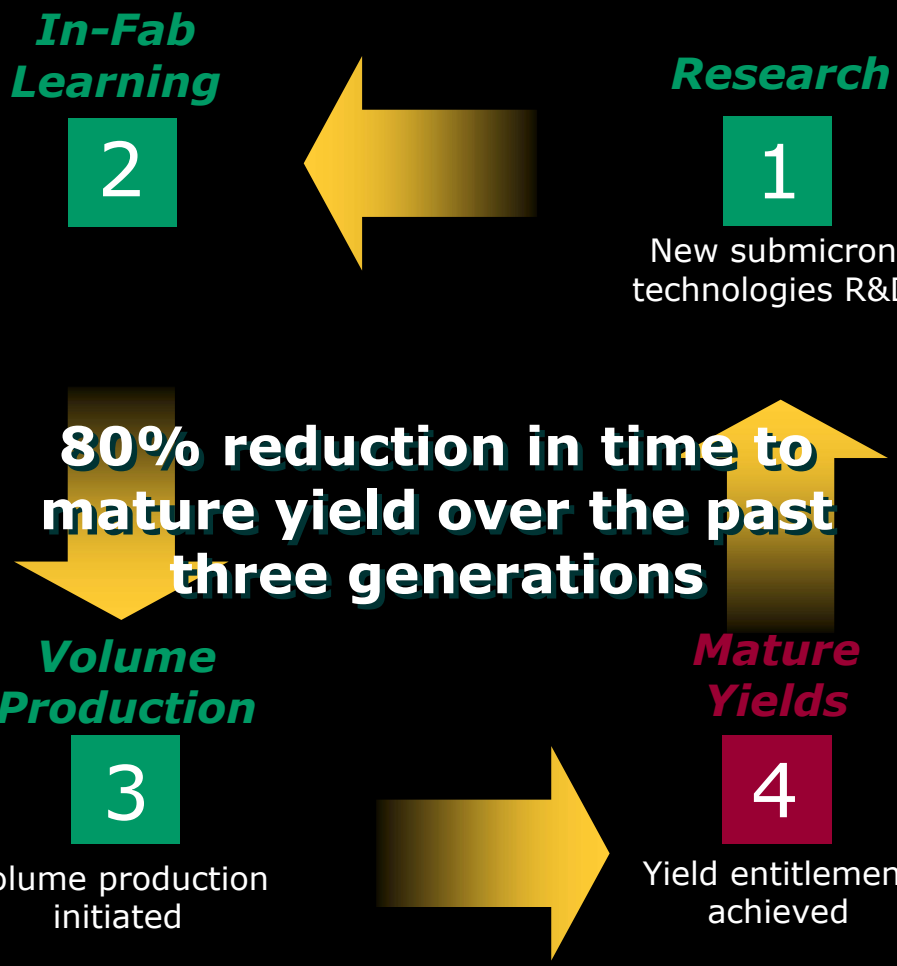
Rapid transition to products in *new* technology generations

- **Fast, smooth transitions using the most advanced submicron structures and materials**
- **Consistent reduction in time to mature yields on new products in the next technology generation**

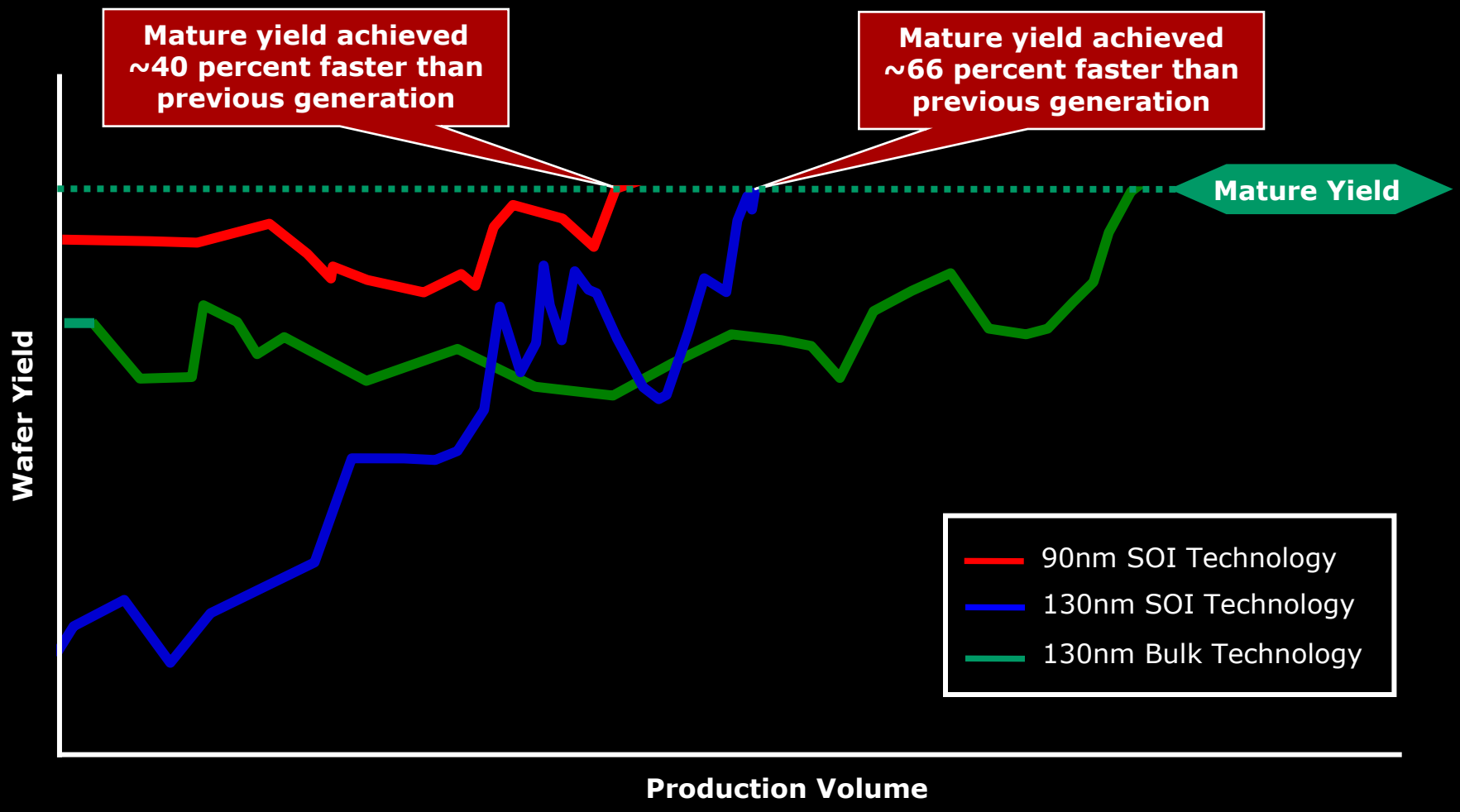
Faster Technology Introduction

APM enables faster transitions to new technology generations and achievement of mature yields

Customers can introduce their latest, highest performing, highest margin products sooner



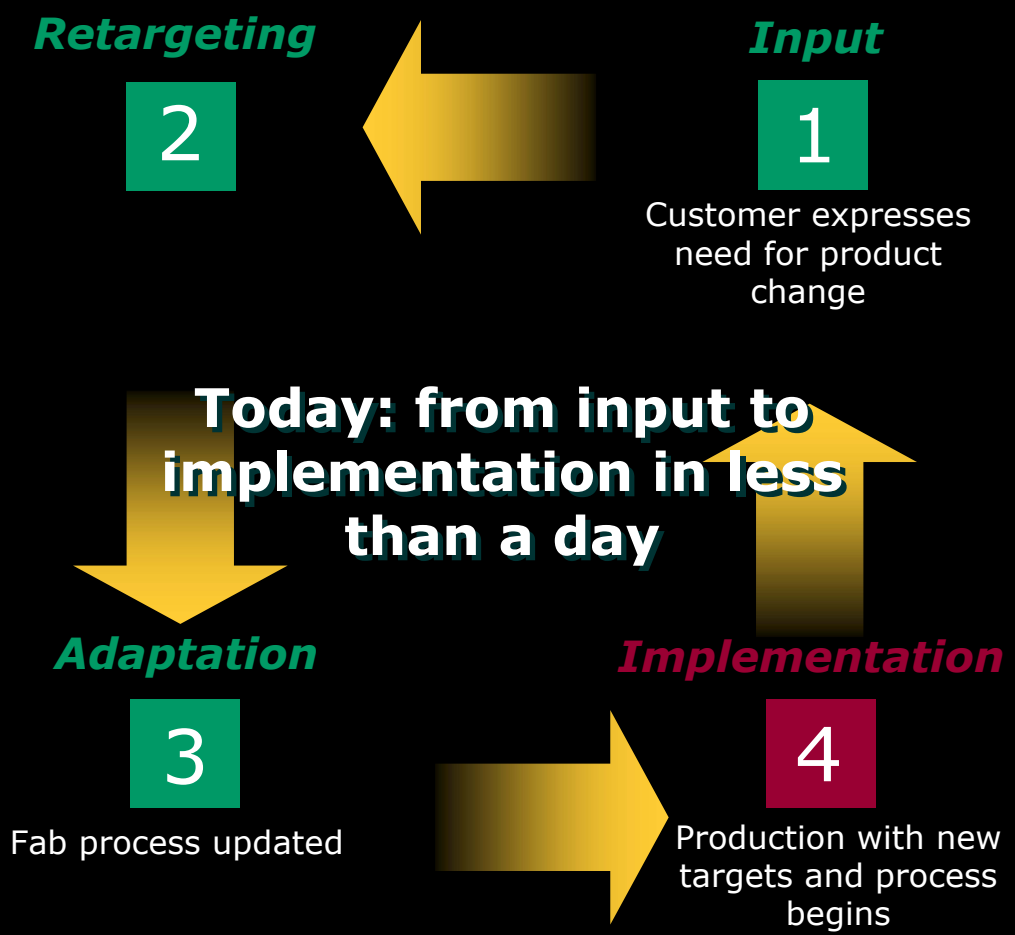
Faster Yield Ramp, Generation After Generation



More Agile Customer Response

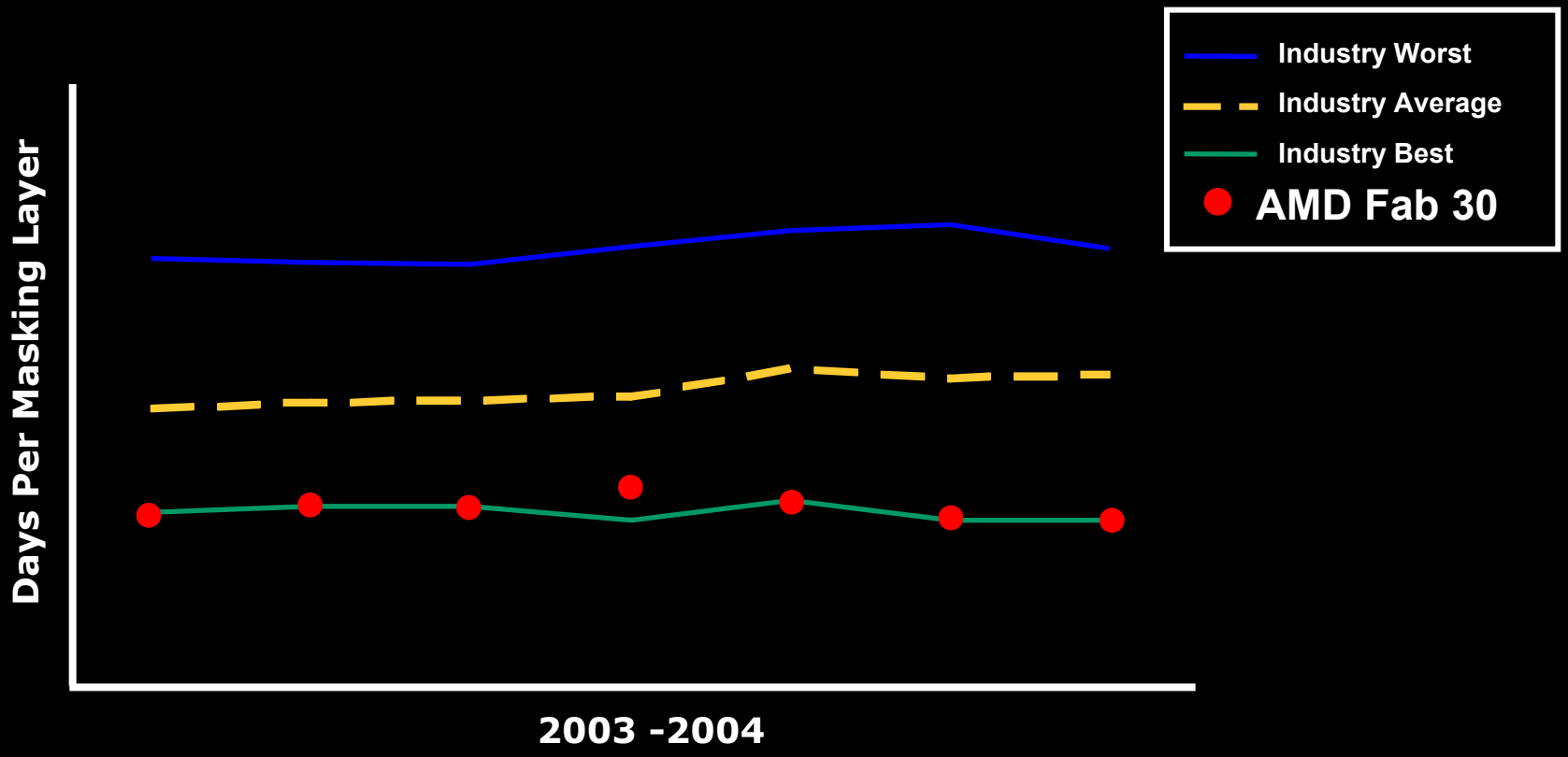
APM enables more agile changes to production mix and product power/performance targets

Customers can more accurately match product supply with demand to take full advantage of near-term revenue opportunities



Faster Processing Cycle Times

Once changes are implemented, APM helps deliver them to customers faster

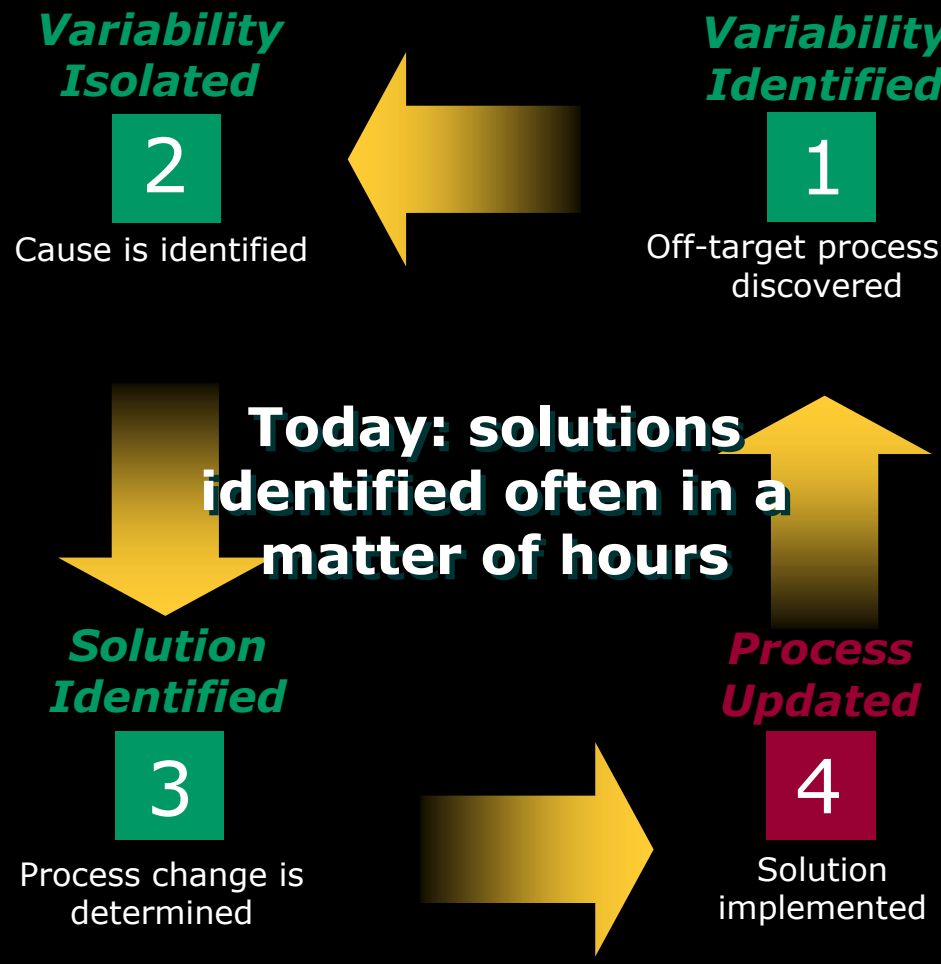


Sources: AMD & Sematech

Better Quality and Higher Efficiencies

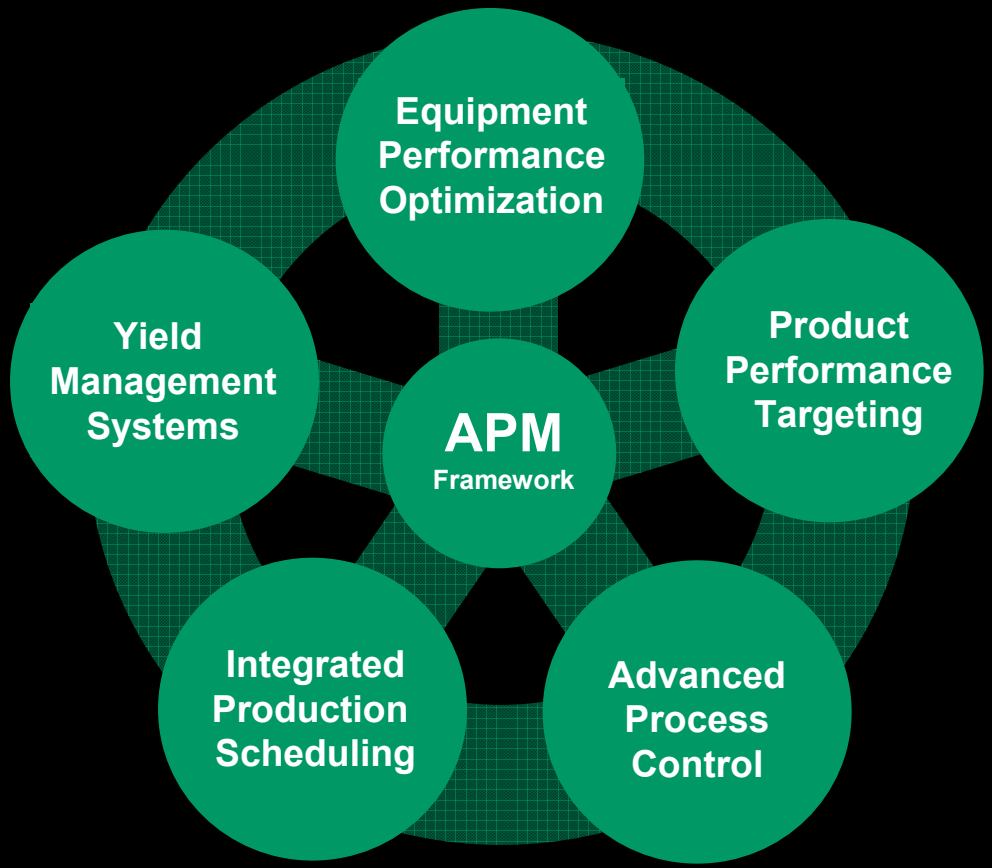
APM enables more accurate identification and correction of processing variability

Customers can better forecast and achieve supply chain requirements due to consistent delivery volumes



APM: Unique Technology Framework

Over 400 AMD patented or patent-pending technologies



Highly automated and synchronized *decision making*

Five integrated algorithmic analysis systems — much more than just APC

Includes proprietary technologies, logic and business processes

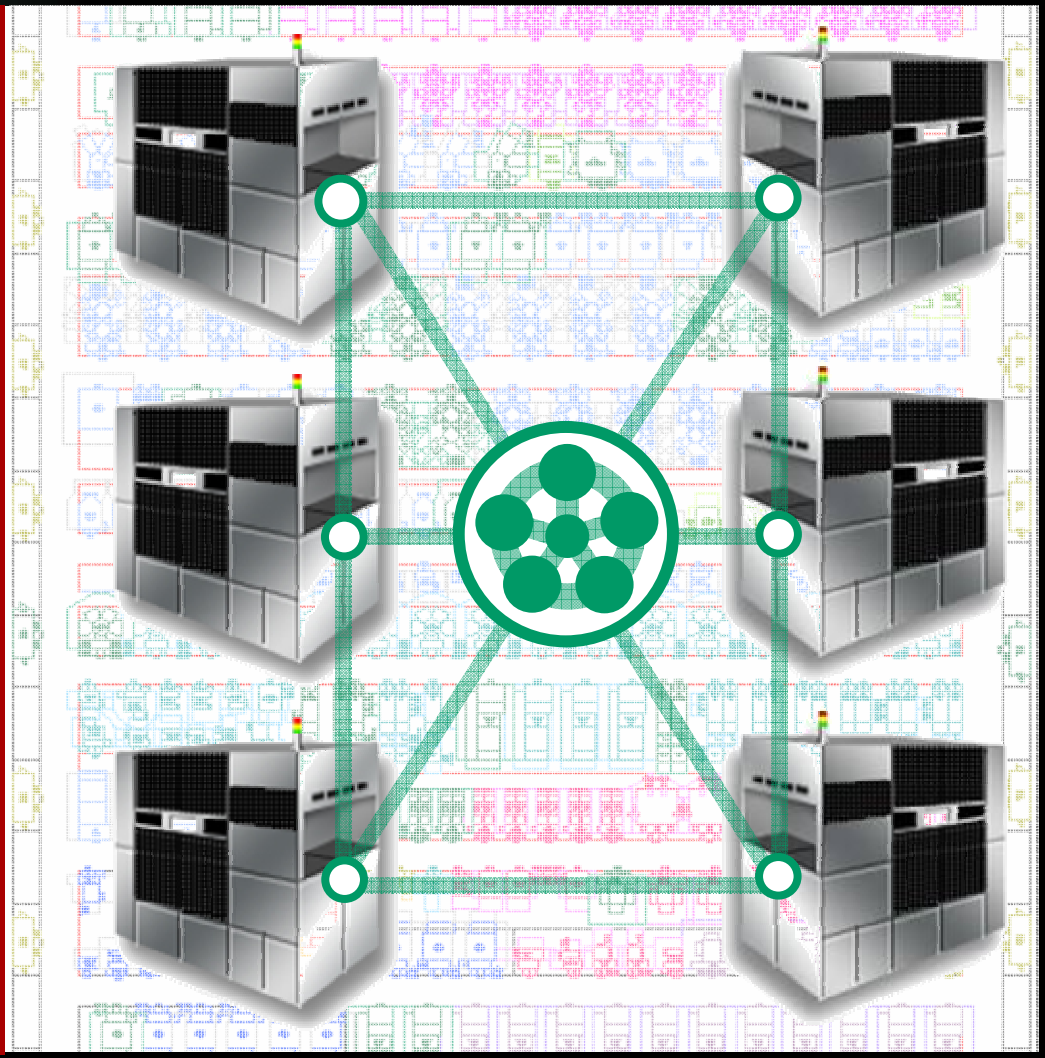
Fed by fab-wide tool and data integration

Fab-Wide Tool and Data Integration

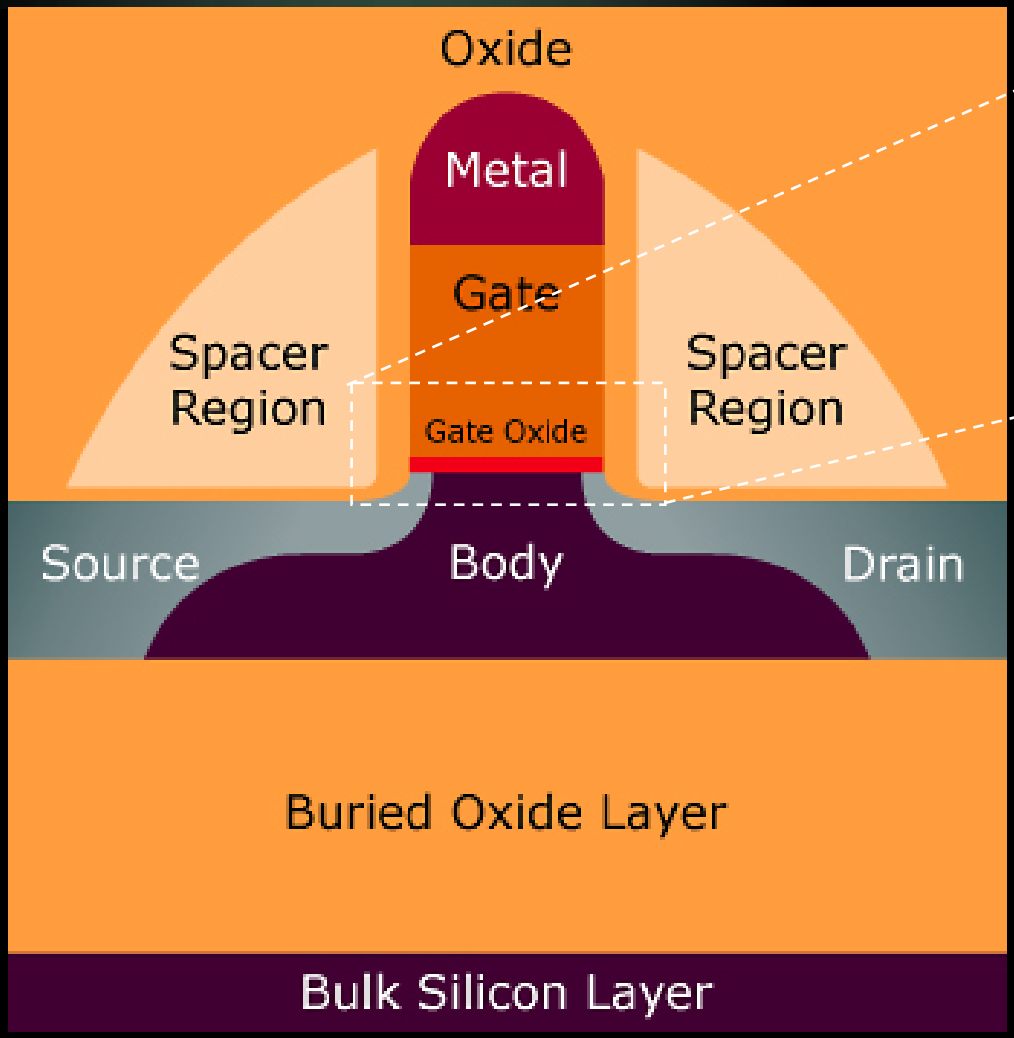
All critical tool sets within AMD fabs are networked and integrated into the APM framework

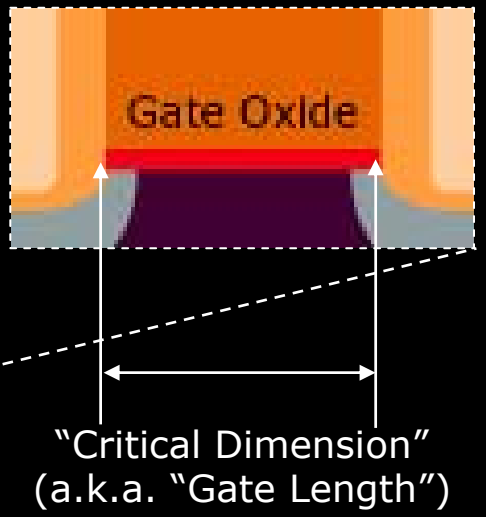
APM constantly monitors the health of all tools as well as the current health of all chips in production

Using this information, APM can automatically adjust chip recipes to account for small but critical changes in tool performance



Example: "Critical Dimension" Control





Adjusting the critical dimension on each transistor results in a performance change in the resulting chip

There are over 200 million transistors in the current dual-core AMD Opteron™ processor

Example: "Critical Dimension" Control

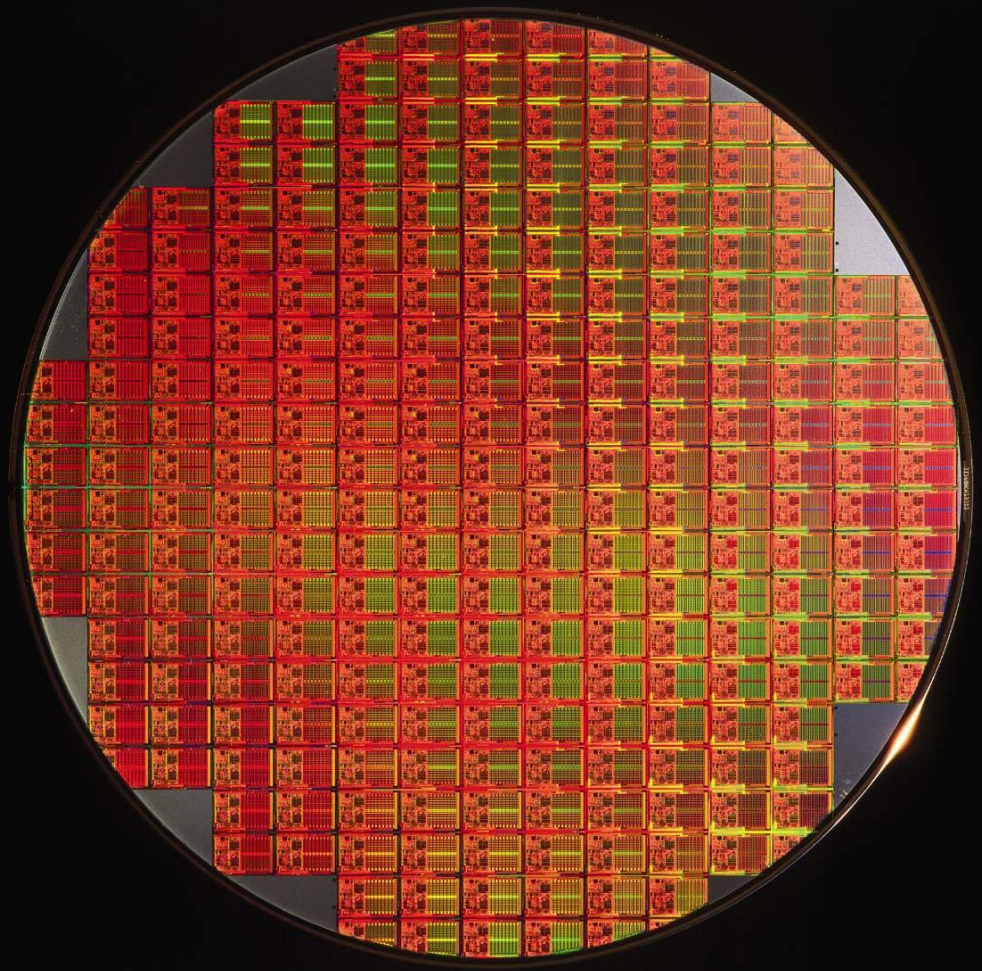
Using APM, AMD can rapidly, accurately and automatically make ***adjustments as small as 1nm*** (60 thousand times smaller than a human hair) to the critical dimension ...

In *every* transistor

In *every* chip

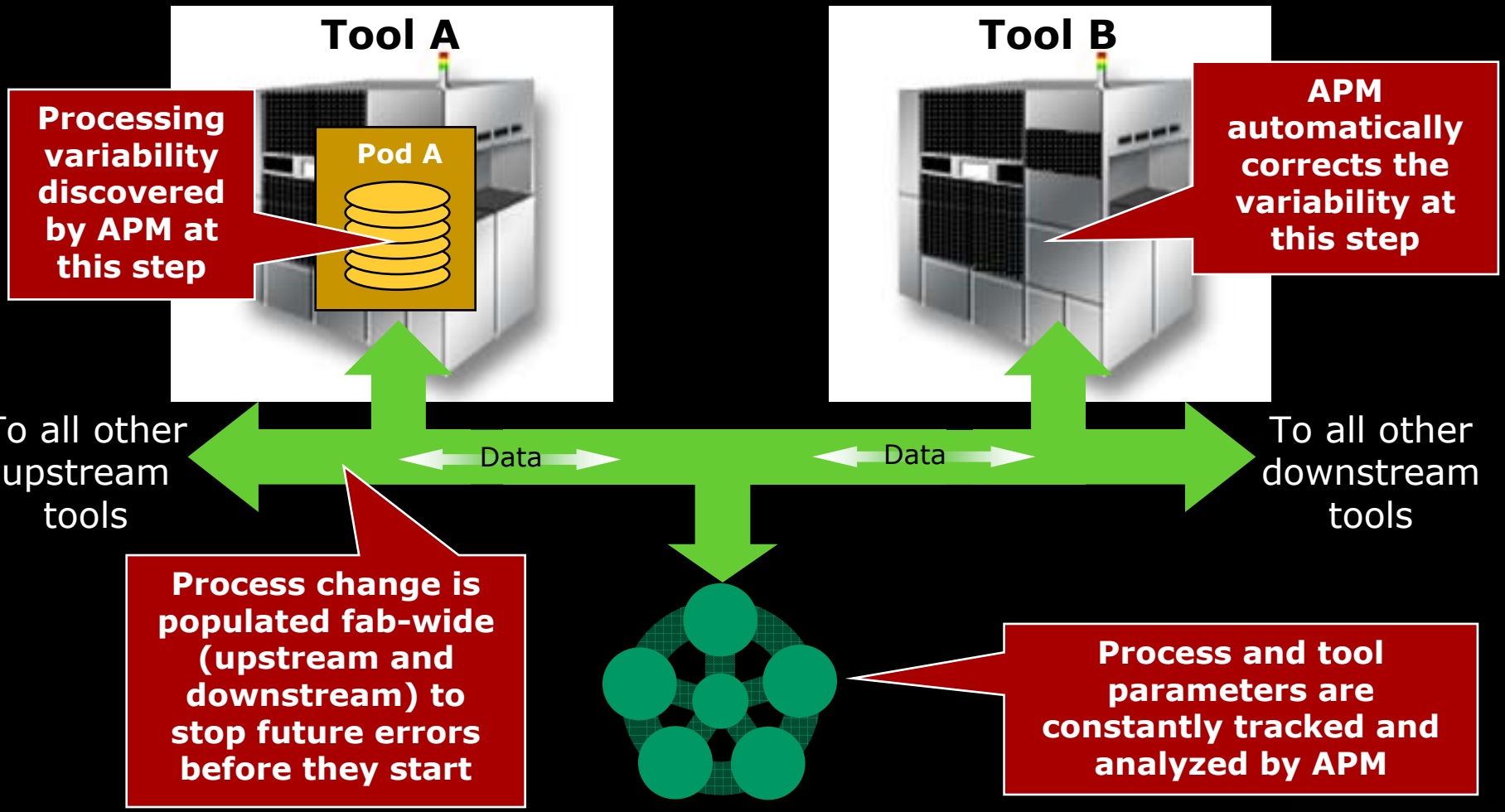
On *every* wafer

That's roughly 21 billion transistors per wafer*



* Based on production of 90nm AMD Opteron processors on 200mm wafers

Example: Feed Forward, Feed Backward Correction

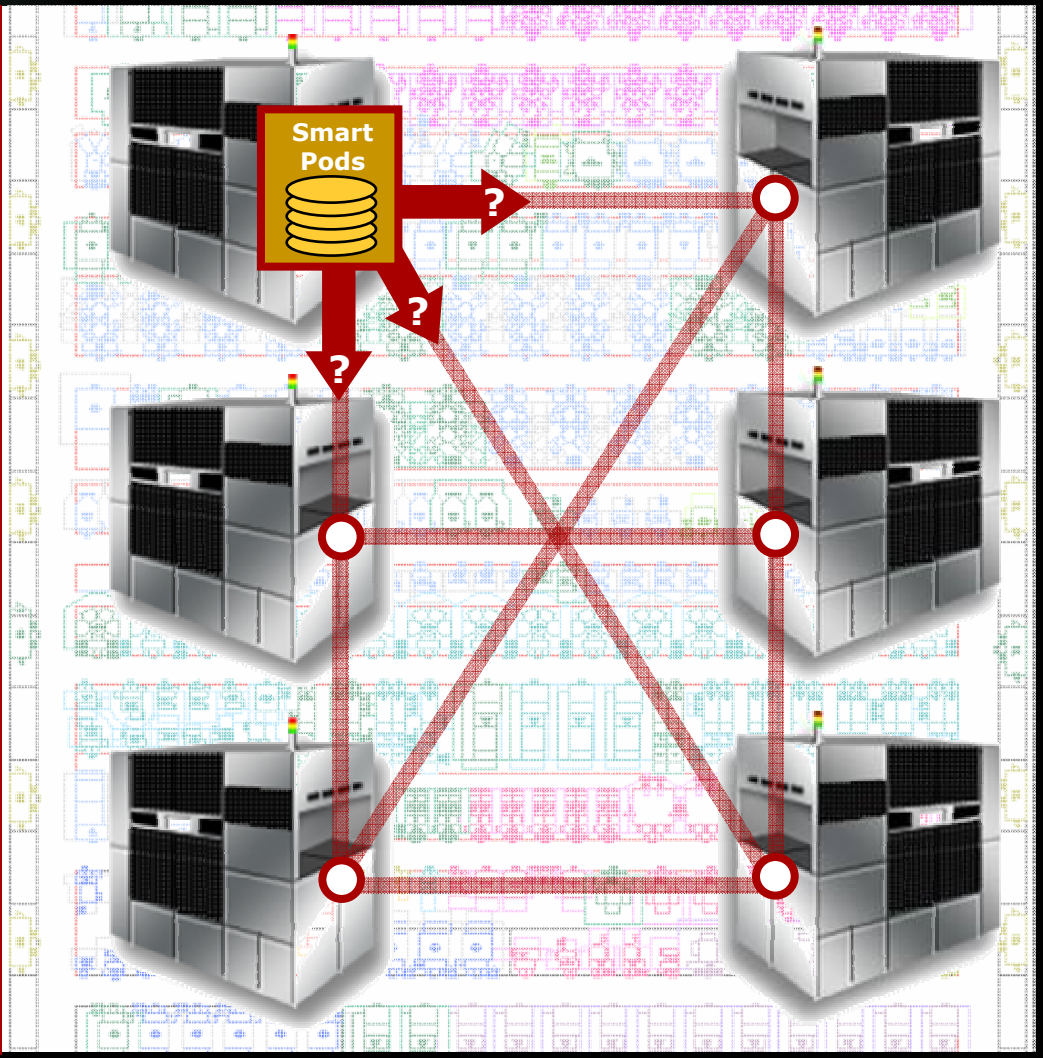


Sneak Peek at APM 3.0: Agent Based Scheduling

Tool to tool automated delivery creates thousands of possible processing paths

Which is the most efficient and cost effective path based on customer requirements?

Software agents are used to enable pod to tool negotiation on the optimal processing path based on current tool and wafer states



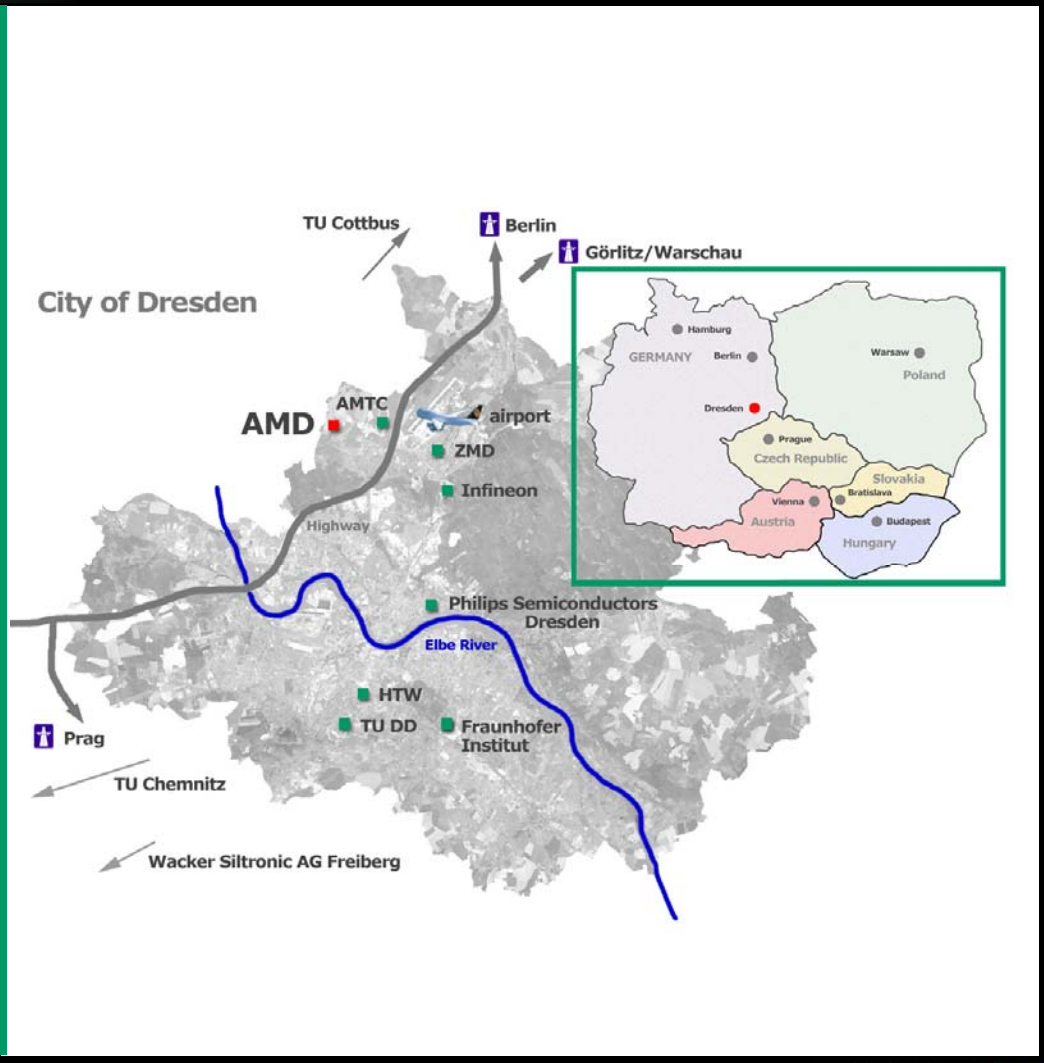
Ongoing Success in Saxony

Dresden: One of Europe's largest microelectronics clusters

Center of operations for AMD microprocessor fabrication

Tremendous ongoing success for AMD, The Free State of Saxony, and Germany

Over 7,000 jobs directly or indirectly created by AMD since 1996



AMD Fab 36: AMD's Next Benchmark Fab

Expected to be the most advanced 300mm fab in the world when completed

First test wafer starts in March 2005
Only 16 months from ground breaking to first silicon
On track for volume production in 2006

Planned for 65nm, 45nm and 32nm technology generations

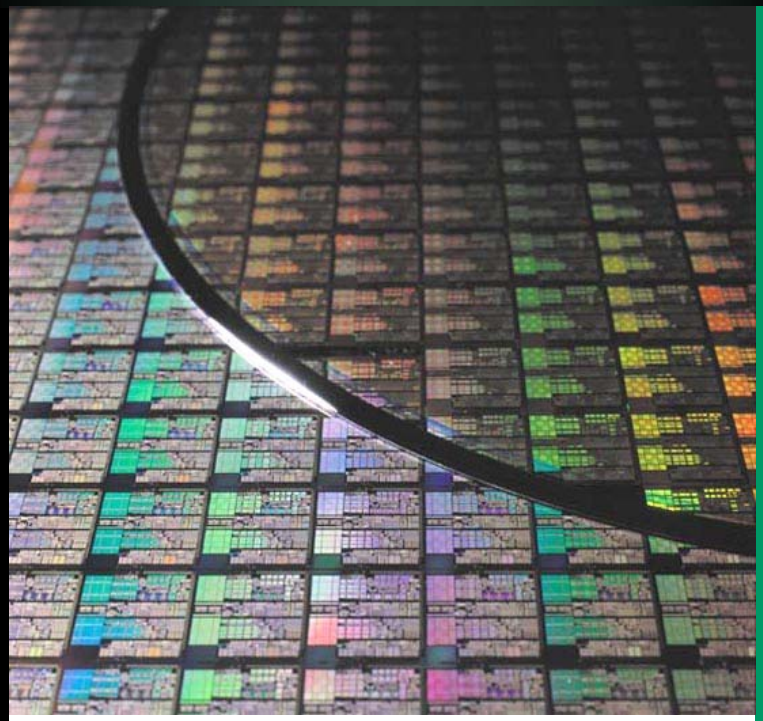
AMD Fab 30: Delivering on the Promise

AMD's flagship 200mm fab today producing all AMD64 and AMD Sempron™ processors

All AMD64 wafer starts converted to 90nm by mid-2005

Dual-core AMD64 processors shipping for revenue

Chartered Agreement

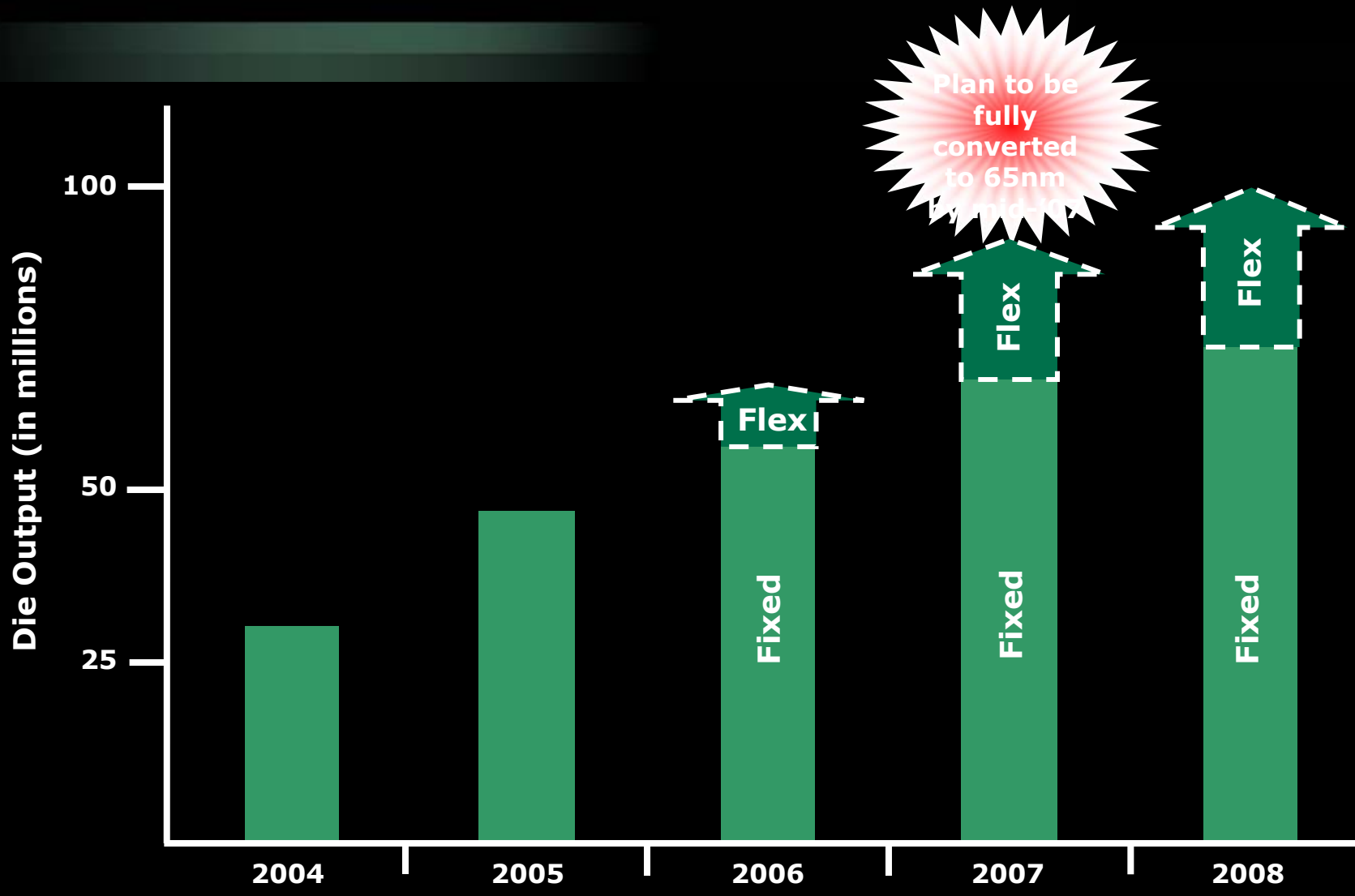


Chartered
semiconductor manufacturing

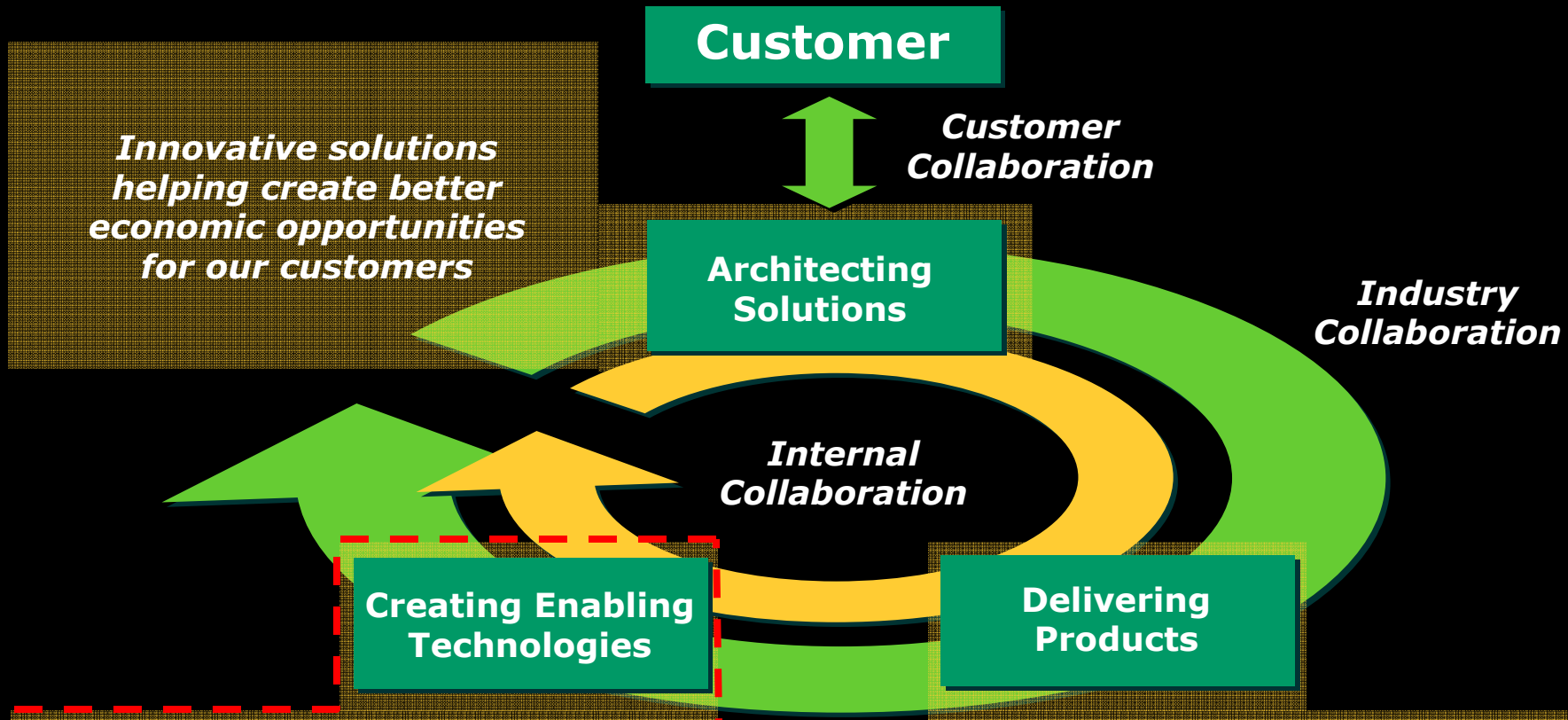
Manufacture of AMD64 microprocessors at Chartered planned to begin in 2006

Operational flexibility — ability to add manufacturing capacity as needed

Executing for Maximum Advantage



Customer-Centric Technology Innovation



Unique Model for Process Technology

Create industry-leading process technologies, using a highly efficient and cost-effective model, to enable industry leading microprocessors.

Distributed Early-Stage Development

- Partnerships
- In-house work
- Consortia
- University work

+

In-Fab Late-Stage Development

- New technologies run in-fab to accelerate learning and yield ramp
- "Mixed mode" manufacturing enabled by APM

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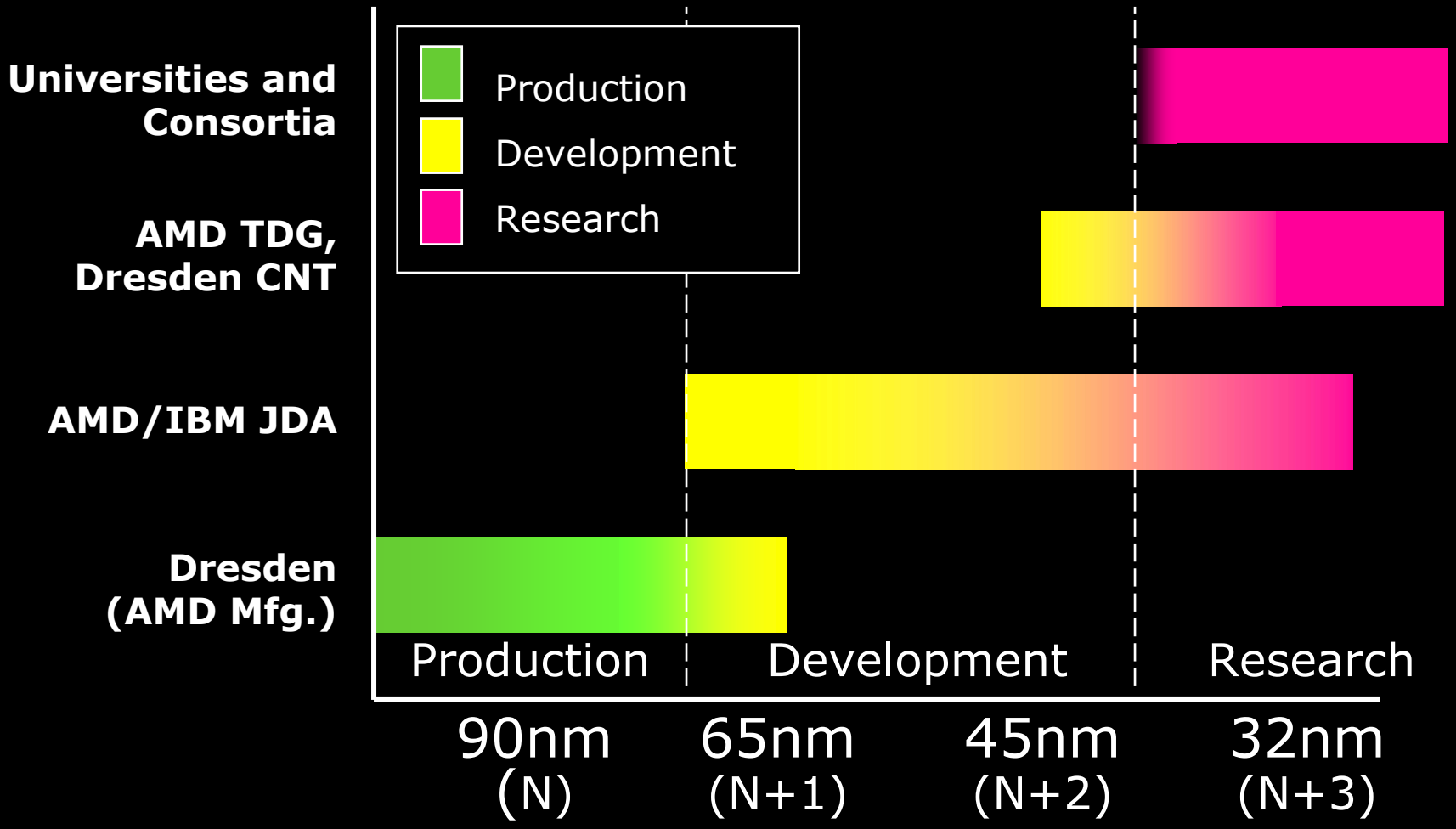
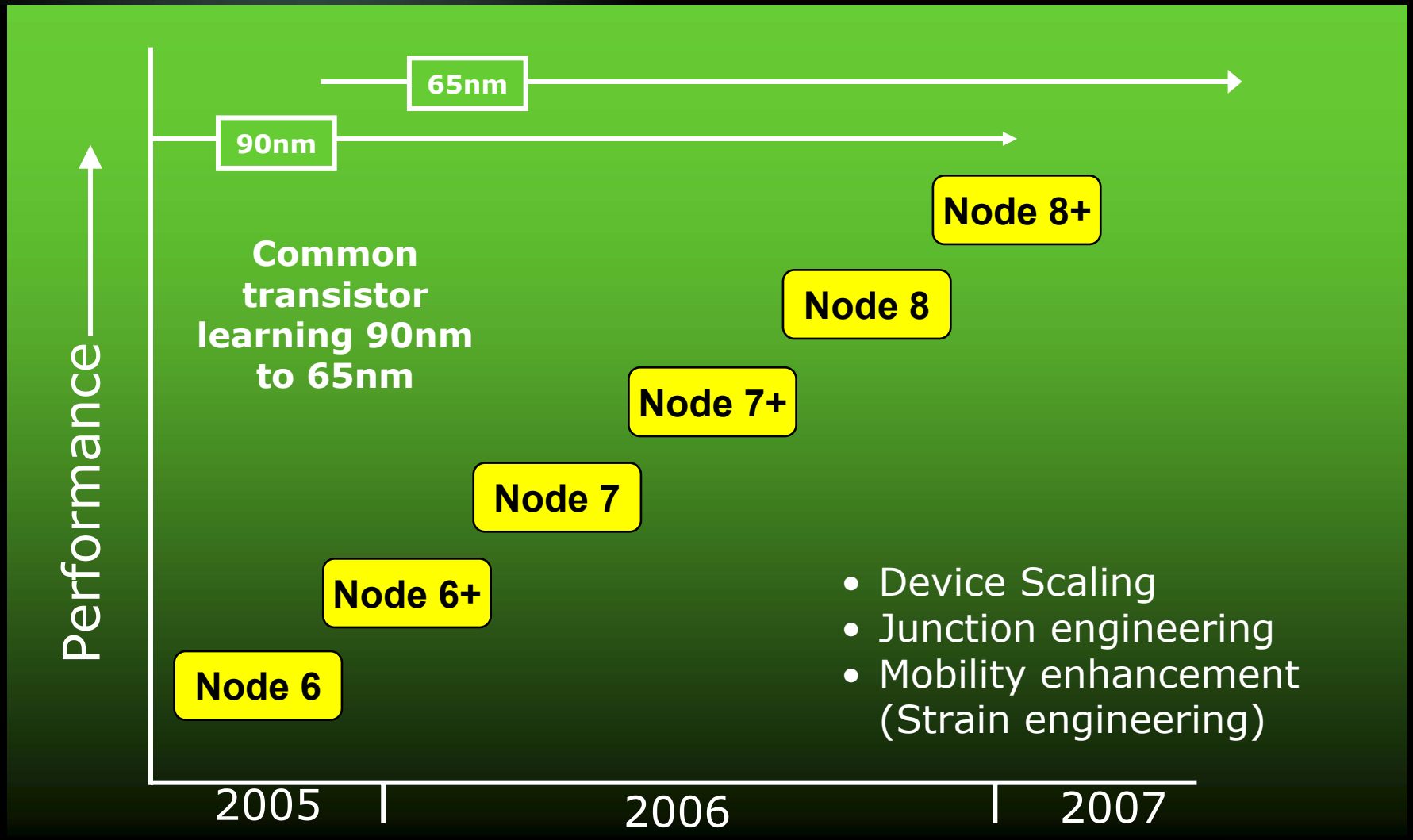
Continuous Technology Improvement

- Quarterly (or more) transistor upgrades
- Rapid, highest value improvements with minimal disruption
- Greatly reduced dependence on major technology generation transitions

Distributed Early Stage Development



Continuous Technology Improvement



Highly Successful 90nm Technology Transition

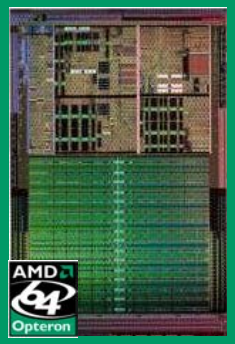
High yield at start of volume production

Builds on 130nm SOI success

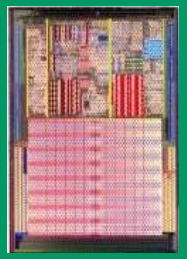
Increased thermal efficiencies

Significant die-size reductions

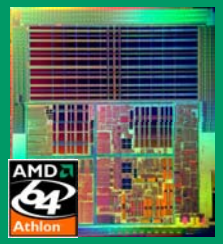
Addition of strained silicon transistor technology



130nm
193mm²



90nm
115mm²



130nm
145mm²

90nm
84mm²

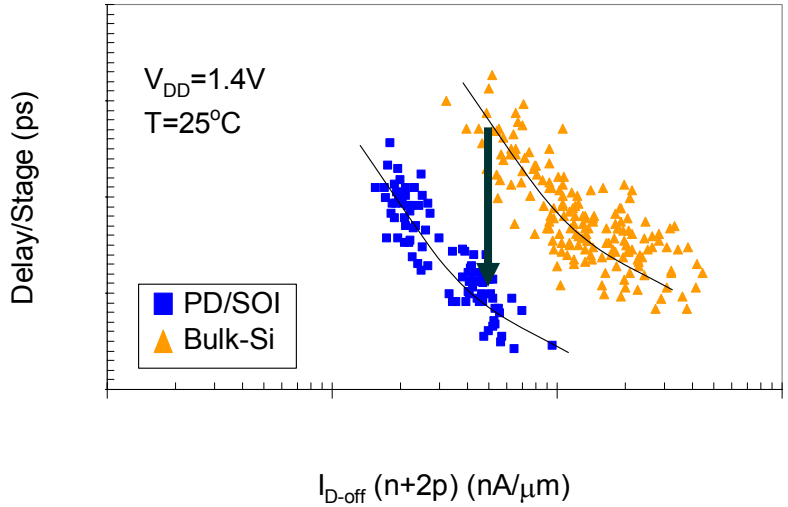
SOI: Dramatically Improved Performance and Power Efficiencies

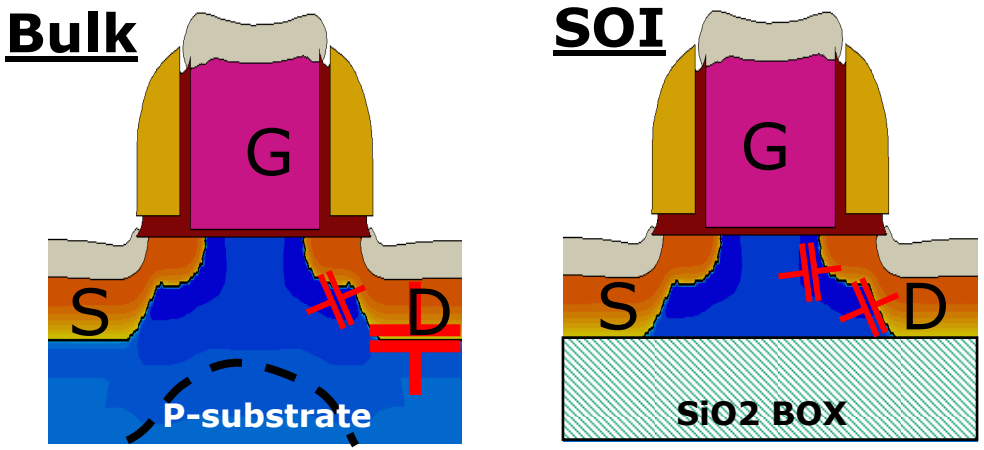
Silicon-on-Insulator Advantages:

At equivalent Off current, SOI can provides up to 18% performance improvement over bulk-Si technology

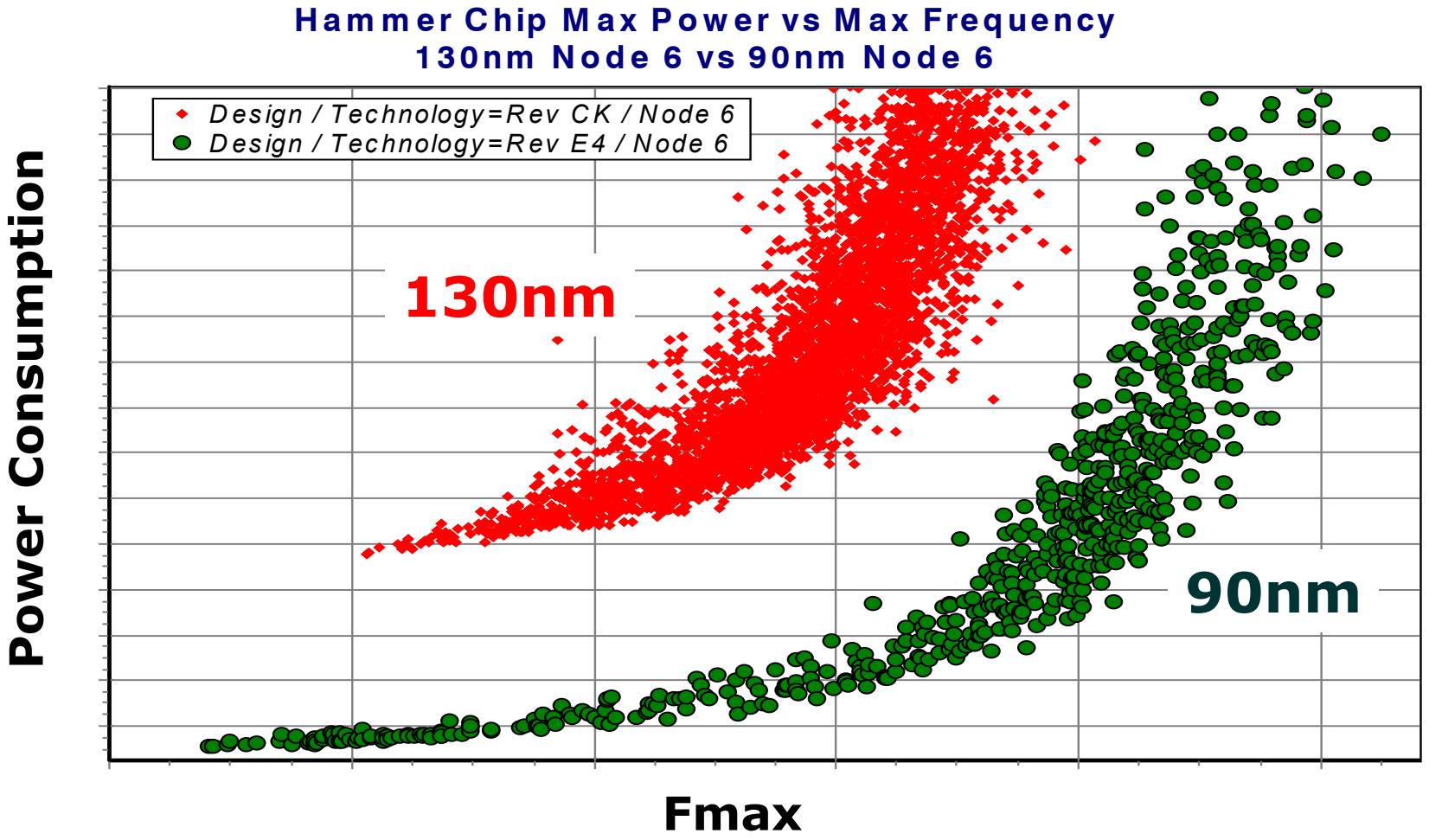
Vertical Cj component is eliminated thus RC delay can be decreased

Higher Reliability due to elimination of latch-up effect and higher radiation hardness





90nm vs 130nm Technology



AMD/IBM Partnership Succeeding

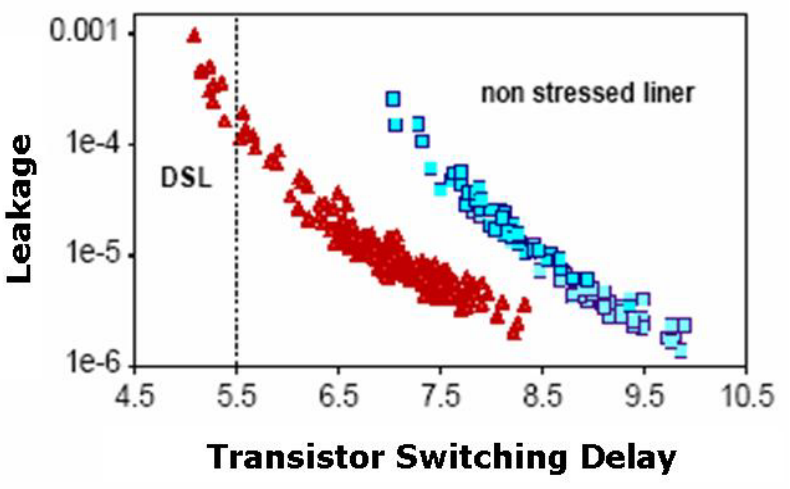
- **Global joint R&D team in Germany and US**
- **Focus on 65nm, 45nm and 32nm technology generations**
- **Germany work taking place at AMD Fab 30 and Fab 36 in Dresden**
- **US work taking place at IBM 300mm facility in East Fishkill, NY**
- **Common goals in high performance**

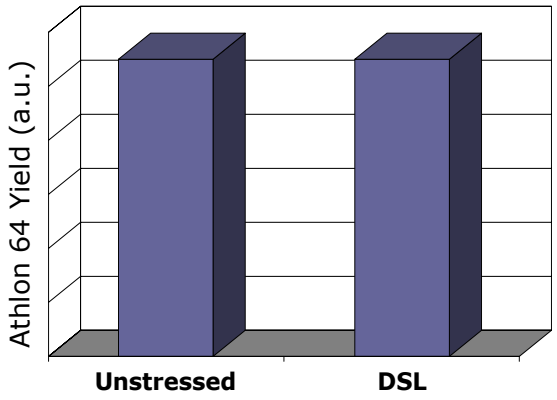
Second-Generation Strained Silicon in Production

~24 percent transistor performance increase with no increase in power

Dual Stress Liners integrated into 90nm generation with equivalent yield

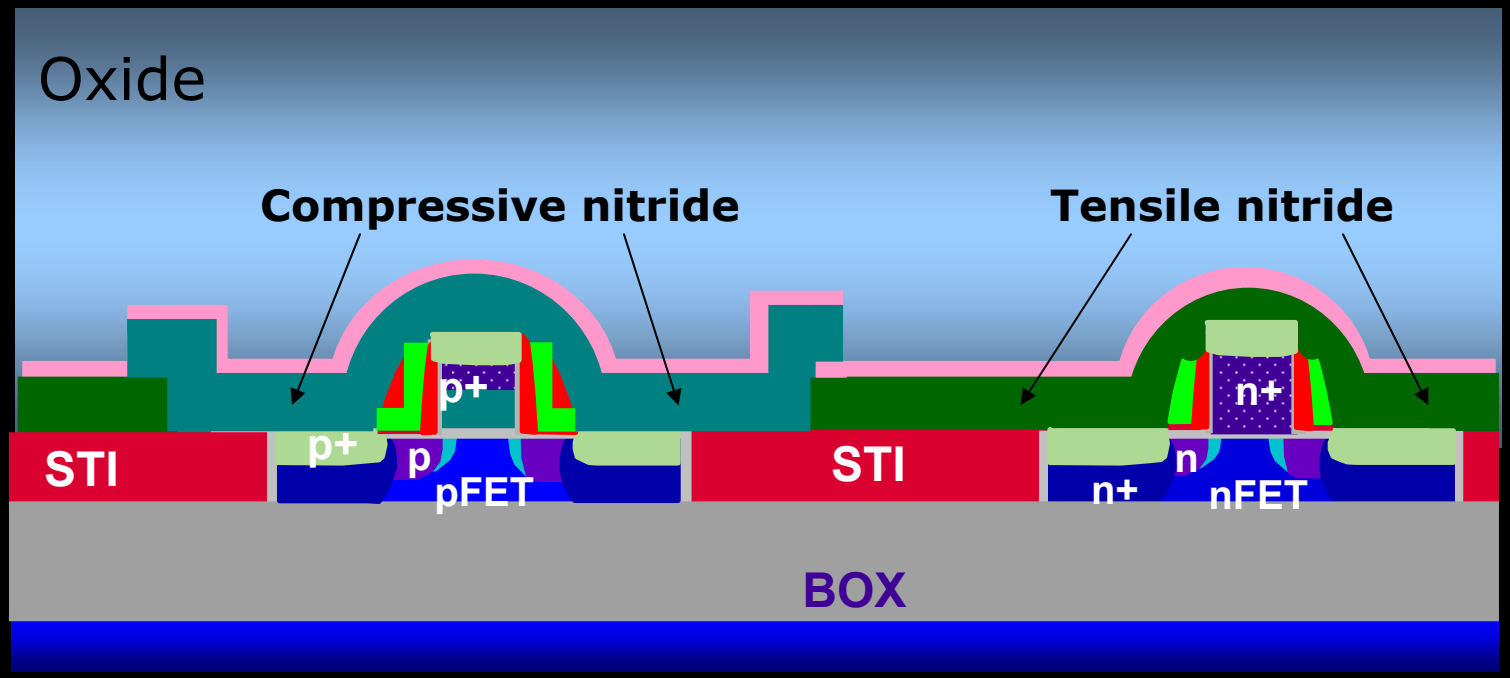
Rapidly integrated into volume manufacturing using standard tools and materials



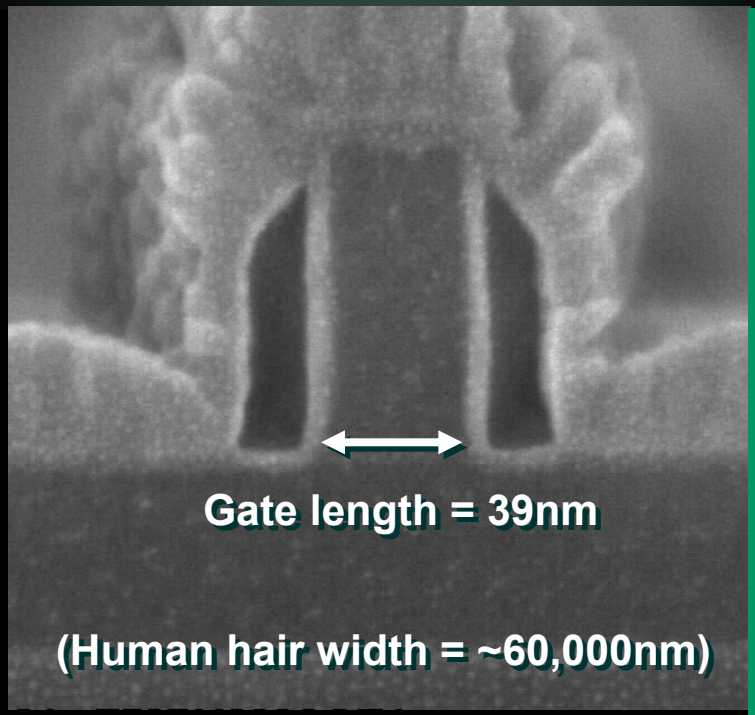


Strain Engineering: Dual Stress Liners (DSL)

Dual Stress Liners simultaneously improve the n-channel and p-channel transistor performance using conventional materials



Great Progress on 65nm Development



High-performance 65nm technology SOI transistor with strain engineering

Achieved our 65nm SRAM milestones

SRAM test vehicle yields are exceeding our development plans

Transistor and interconnect development on schedule

Yield metrics exceeding development plan
3rd generation of strained-silicon
Addition of Nickel Silicide
4th generation of low-k dielectric stack

On schedule for development process installation in Fab 36 in mid-2005

AMD is optimizing Fab 36 for smooth transition of 65nm technology

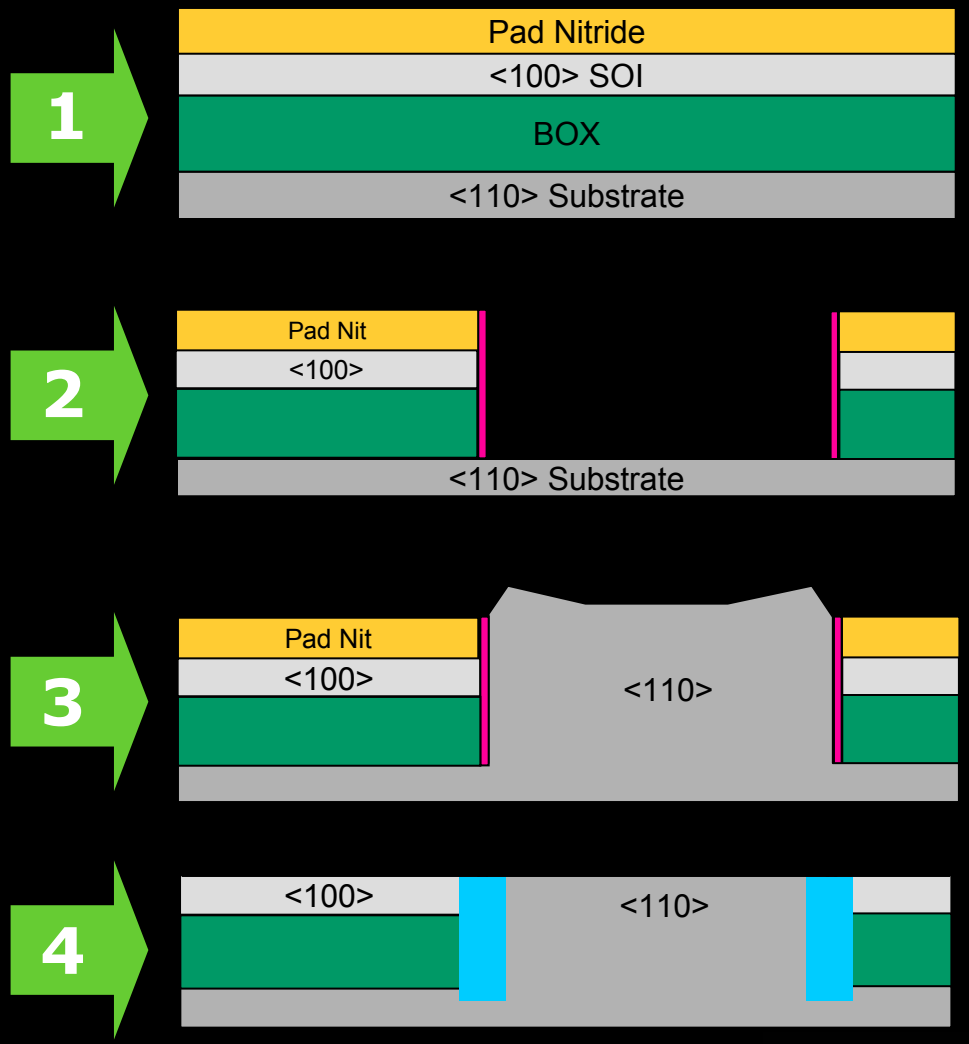
45nm Development On Track

Hybrid Orientation Technology

Developed under ASTA alliance

Mobility improvement using optimal crystal orientation

40-60% enhancement in PFET performance



Post-45nm Research Begun and Progressing

Key candidates:

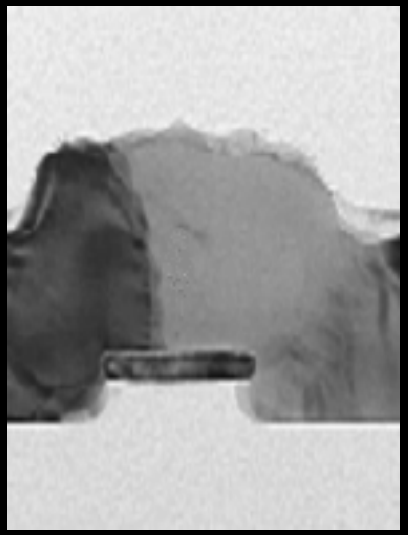
- Ultra-thin, fully-depleted (FDSOI)
- Metal gate (NiSi)
- Intrinsic channels
- Multi-gate 3D structure
- Strain engineering

Expected advantages:

- Lower leakage (Off current and gate leakage)
- Higher drive currents
- Faster switching
- Exceeded ITRS performance projected for 2009

AMD Metal-Gate FDSOI

First Published at SSDM 2003



Multi-gate structure Lg=20 nm

Research transistors surpass ITRS 2009 performance projections

Positioned for Continued Growth and Success

With industry-leading capabilities, accurately aligned capacity levels and world-class execution, AMD is strongly positioned to achieve its aggressive growth objectives through the end of this decade

- APM continues to increase our manufacturing speed, accuracy and agility, enabling us to more rapidly and effectively respond to the needs of customers
- Through smart capacity growth, comprised of both fixed and flexible capacity, AMD can fully achieve its growth objectives and expand capacity as necessary should demand exceed projections
- The Dresden success story continues, with unprecedented levels of efficiency in AMD Fab 30 and the ramp of AMD Fab 36 right on track
- The IBM joint technology alliance is exceeding development objectives and timelines

Cautionary Statement

These presentations contain forward-looking statements, which are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act of 1995. Investors are cautioned that forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from current expectations. Forward-looking statements in these presentations relate to, among other things, the company's anticipated product and technology introduction schedules; and the company's plans for tooling and financing its planned wafer fabrications facility AMD Fab 36. Risks include the possibility that global business and economic conditions will worsen in 2005 resulting in lower than currently expected sales; that Intel Corporation's pricing, marketing programs, product bundling, new product introductions or other activities targeting the company's processor business will prevent attainment of the company's current sales plans; that demand for personal computers and other processor-based products and, in turn, demand for the company's processors will be lower than currently expected; that adoption of AMD64 products by OEMs will not occur as expected; that the company will not be able to meet demand for its products; that the company may not achieve its current product and technology introduction schedules; that technology partners will discontinue collaborating with the company; that the company will not be able to raise sufficient capital to enable it to establish leading-edge capacity to maintain its market leadership positions; that the company may not be able to penetrate further into emerging markets; and that solutions providers will not timely provide the infrastructure, including operating systems and applications, to support the company's AMD64 technology.

Because the company's actual results may differ materially from its plans and expectations today, we encourage you to review the company's filings with the Securities and Exchange Commission, including but not limited to our Annual Report on Form 10-K for the year ended December 26, 2004, and our Quarterly Report on Form 10-Q for the quarter ended March 27, 2005.

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